

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Tajuki YOSHIDA

Appl. No. Unassigned

Filed: December 8, 2003

For: EEPROM WRITING METHOD

Art Unit: 2824

Examiner: Son T. Dinh

Atty. Docket No.: 31869-198458

Customer No.:

26694

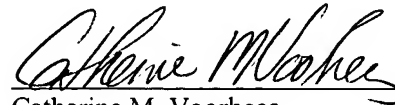
INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In accordance with the duty of disclosure under 37 CFR § 1.56, Applicant hereby notifies the U.S. Patent and Trademark Office of the documents that are listed on the attached PTO-1449 forms. All of the listed references are of record in parent Application No. 10/119,124, where copies may be obtained in accordance with customary U.S. Patent and Trademark Office practice. Applicant requests that these documents be considered and listed on the face of any patent granted in this application.

Respectfully submitted,



Catherine M. Voorhees
Registration No. 33,074

VENABLE

P.O. Box 34385
Washington, D.C. 20043-9998
Telephone: (202) 344-4000
Telefax: (202) 344-8300

Date: December 8, 2003

CMV/elw
DC2/503343

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT				Atty Docket: 31869-178950		Application No.: Rule 53(b) Divisional of Application No. 09/680,315	
				Applicant Takuji YOSHIDA		<div style="display: flex; align-items: center; justify-content: center;"> <div style="writing-mode: vertical-rl; transform: rotate(180deg); font-weight: bold; margin-right: 5px;"> J1036 U.S. PRO 10/119124 </div> <div style="writing-mode: vertical-rl; transform: rotate(180deg); font-weight: bold; margin-left: 5px;"> 04/10/02 </div> </div>	
				Filing Date Concurrently			
U.S. PATENT DOCUMENTS							
Examiner Initial	Document Number	Date	Name	Class	Sub-Class	Filing Date	
CN	AA	4,503,524	McELROY				
CN	AB	4,769,787	FURUSAWA et al.				
CN	AC	4,953,928	ANDERSON et al.				
CN	AD	5,022,000	TERASAWA et al.				
CN	AE	5,047,981	GILL et al.				
CN	AF	5,077,691	HADDAD et al.				
CN	AG	5,122,985	SANTIN				
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CN	AH	5494	01/12/1984	JAPAN			
CN	AI	52300	02/28/1989	JAPAN			
	AJ						
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
CN	AK	D'ARRIGO et al., 1989 IEEE International Solid-State Circuits Conference, pp. 132-133; Session 10: Non-Volatile Memories; Tham 10.3: "A 5V-Only 256k Bit CMOS Flash EEPROM."					
CN	AL	N. ANANTHA et al., "Electrically Erasable Floating Gate F.E.T. Mem. Cell," IBM Tech. Discl. Bull., Vol. 17, No. 8, Jan. 1975, pp. 2311-2313.					
CN	AM	R. DOCKERTY, "Nonvol. Mem. Array w. Single Famos Dev. Per Cell," IBM Tech. Discl. Bull., Vol. 17, No. 8, Jan. 1975, pp. 2314-2315.					
CN	AN	M. KIKUCHI et al., "A 2047-Bit-N-Channel Fully Decoded Electrically Writable/Erasable Nonvol. R.O.M.," "1 ST European Solid State Circuits Conf. (ESSIRC) Kent, England, Sept. 2-5, 1975, pp. 66-67.					
Examiner SON DINH						Date Considered 10/20/02	
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							

FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT			Atty Docket: 31869-178950		Rule 53(b) Divisional of Application No. 09/680,315		
			Applicant Takuji YOSHIDA				
			Filing Date Concurrently		Group Art: 2824		
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub- Class	Filing Date
	AA	5,134,449	7/1992	GILL et al.			
	AB	5,146,106	9/1992	ANDERSON et al.			
	AC	5,155,701	10/1992	KOMORI et al.			
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	AE	5,177,705	1/1993	McELROY et al.			
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	AG	5,235,544	10/1993	CAYWOOD			
	AH	5,265,052	11/1993	D'ARRIGO et al.			
	AI	5,003,510	3/1991	KAMISAKI			
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	AJ						
	AK						
	AL						
OTHER (Including Author, Title, Date, Pertinent Pages, etc.)							
	AM						
	AN						
Examiner					Date Considered		
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				Filing Date Concurrently		Group Art: 2824	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub- Class	Filing Date
SN	AA	5,781,476	7/14/1998	SEKI et al.			
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SN	AH	0 320 231	6/14/1989	Europe			
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	AN	Haddad, et al., "Degradations Due to Hole Trapping in Flash Memory Cells", IEEE Electron Device Letters, Vol. 10, No. 3, March 1989, pp. 117-119.					
	AO						
Examiner SON DINH					Date Considered 10/28/02		
EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.							

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				Filing Date Concurrently		Group Art: 2824	
U.S. PATENT DOCUMENTS							
Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date
	AA	4,823,318	4/1989	D'ARRIGO et al.			
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	AH						
	AI						
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	AK	01-021795	01/25/1989	JP			
	AL	62-099997	05/09/1987	JP			
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	AM						
	AN						
Examiner					Date Considered		
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31869-178950

[illegible][illegible]Date
Considered

SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

VENABLE

Notice of References Cited

Application/Control No.

10/119,124

Applicant(s)/Patent Under
Reexamination
YOSHIDA, TAKUJI

Examiner

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Art Unit

2824

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6392933	05-2002	Yoshida	365/185.29
	B	US-			
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.